In-System Programming Times for MAX Devices

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Application Note 85

Introduction

In-system programmability (ISP) offers advantages for programmable logic users throughout the life of their products. In the prototyping stage, design revisions can be compiled and programmed in the device within minutes. During production, ISP simplifies the manufacturing flow by allowing devices to be programmed during board test with in-circuit testers. Systems that use ISP-capable devices can be easily upgraded in the field by downloading new configurations via modem or other data links.

The time required to program a device in-system is important, especially during manufacturing. Altera® MAX® 9000 (including MAX 9000A), MAX 7000S, and MAX 7000A devices are programmed in-system through the IEEE 1149.1 Joint Test Action Group (JTAG) interface. These devices can be programmed using the following methods:

- With an adaptive programming algorithm for the fastest possible programming times.
- With a fixed or constant programming algorithm for platforms that cannot support adaptive algorithms. These devices are marked with an “F” suffix.

Information on MAX 7000A devices is preliminary. Contact Altera Applications at (800) 800-EPLD for the most up-to-date information.

The ISP process involves the shifting of addresses and data for both programming and verification. The maximum clock frequency supported by MAX 9000, MAX 7000S, and MAX 7000A programming via the IEEE 1149.1 JTAG port is 10 MHz. The total time needed to program a device in-system consists of the time required to shift address and data information along with the time to program and verify the EEPROM cells. For these devices, fast data throughput rates result in very short in-system programming times.

This application note describes the programming sequence, how to calculate programming and verification times, and several programming methods.

Programming Sequence

During in-system programming, instructions, addresses, and data are shifted into the device through the TDI input pin. Data is shifted out through the TDO output pin and compared against the expected data.

Programming a pattern into the device requires the following six ISP stages. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6.

1. *Enter ISP*. The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode. The enter ISP stage requires 1 ms.

2. *Check ID*. Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.

3. *Bulk Erase*. Erasing the device in-system involves shifting in the instructions to erase the device and applying one erase pulse of 100 ms.

4. *Program*. Programming the device in-system involves shifting in the address and data and then applying the programming pulse to program the EEPROM cells. This process is repeated for each EEPROM address.

5. *Verify*. Verifying an Altera device in-system involves shifting in addresses, applying the read pulse to verify the EEPROM cells, and shifting out the data for comparison. This process is repeated for each EEPROM address.

6. *Exit ISP*. An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode. The exit ISP stage requires 1 ms.

Programming Times

The time required to implement each of the six programming stages can be broken into the following two elements:

- A pulse time to erase, program, or read the EEPROM cells.
- A shifting time based on the test clock (TCK) frequency and the number of TCK cycles to shift instructions, address, and data into the device.

By combining the fixed and variable times for each of the six programming stages, you can determine the time needed to program or verify a device as a function of the TCK frequency, the number of devices, and the target device. Because different ISP-capable devices have a different number of EEPROM cells, both the total fixed and total variable times are unique for the selected device. The pulse time for "F"-suffix devices are screened to a pre-selected value and therefore, are known prior to programming. The pulse time for the adaptive algorithm (i.e., non-"F" devices) varies from device to device. On average, however, this pulse is much shorter than for "F" devices.

The following section discusses the time required to program a single device, concurrently program multiple devices in an IEEE 1149.1 JTAG chain, and bypass devices not targeted for ISP.

Programming a Single Device

The time required to program a single device in-system can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \frac{Cycle_{PTCK}}{f_{TCK}}$$

where: t_{PROG} = Programming time
t_{PPULSE} = Sum of the fixed times to erase, program, and verify the EEPROM cells
$Cycle_{PTCK}$ = Number of TCK cycles to program a device
f_{TCK} = TCK frequency

The ISP times for a stand-alone verification of a single device can be calculated from the following formula:

$$t_{VER} = t_{VPULSE} + \frac{Cycle_{VTCK}}{f_{TCK}}$$

where: t_{VER} = Verify time
t_{VPULSE} = Sum of the fixed times to verify the EEPROM cells
$Cycle_{VTCK}$ = Number of TCK cycles to verify a device

Table 1 lists the t_{PPULSE}, t_{VPULSE}, $Cycle_{PTCK}$, and $Cycle_{VTCK}$ values for MAX 9000, MAX 7000A, and MAX 7000S devices.

Table 1. MAX 9000 & MAX 7000S T_{PPULSE} & $Cycle_{TCK}$ Values

Device Family	Device	Programming		Stand Alone Verification	
		t_{PPULSE} (s)	$Cycle_{PTCK}$	T_{VPULSE} (s)	$Cycle_{VTCK}$
MAX 9000	EPM9560, EPM9560A	12.01	2,2423,00	0.15	981,540
	EPM9480, EPM9480A	11.83	2,243,00	0.15	981,540
	EPM9400	11.65	2,059,00	0.15	907,570
	EPM9320, EPM9320A	11.46	1,875,000	0.15	833,600
MAX 7000S	EPM7256S	6.43	1,384,000	0.03	860,000
	EPM7192S	5.71	1,089,000	0.03	672,000
	EPM7160S	5.38	922,500	0.03	722,000
	EPM7128S	5.11	775,000	0.03	480,000
	EPM7064S	4.57	480,000	0.03	292,000
	EPM7032S	4.30	332,500	0.03	198,000
MAX 7000A	EPM71024A	2.95	1,183,00	0.06	598,000
	EPM7512A	2.95	593,000	0.06	300,000
	EPM7384A	2.95	446,000	0.06	225,000
	EPM7256A	6.43	1,384,000	0.03	860,000
	EPM7128A	5.11	775,000	0.03	480,000
	EPM7064A	2.95	70,000	0.06	35,000
	EPM7032A	2.95	35,000	0.06	18,000

Tables 2 and 3 show the in-system programming and stand alone verification times for several common test clock frequencies.

Table 2. In-System Programming Times for Different Test Clock Frequencies (Part 1 of 2)

Device Family	Device	f_{TCK}								Units
		10 MHz	5 MHz	2 MHz	1 MHz	500 kHz	200 kHz	100 kHz	50 kHz	
MAX 9000	EPM9560, EPM9560A	12.25	12.49	13.22	14.43	16.85	24.12	36.24	60.47	s
	EPM9480, EPM9480A	12.05	12.27	12.95	14.07	16.31	23.04	34.26	56.69	s
	EPM9400	11.85	12.06	12.67	13.70	15.76	21.94	32.24	52.83	s
	EPM9320, EPM9320A	11.65	11.84	12.40	13.34	15.21	20.84	30.21	48.96	s

Table 2. In-System Programming Times for Different Test Clock Frequencies (Part 2 of 2)

Device Family	Device	f_{TCK}								Units
		10 MHz	5 MHz	2 MHz	1 MHz	500 kHz	200 kHz	100 kHz	50 kHz	
MAX 7000S	EPM7256S	6.57	6.71	7.13	7.82	9.20	13.35	20.27	34.11	s
	EPM7192S	5.82	5.93	6.26	6.80	7.89	11.16	16.60	27.49	s
	EPM7160S	5.47	5.57	5.84	6.30	7.23	9.99	14.61	23.83	s
	EPM7128S	5.19	5.27	5.50	5.89	6.66	8.99	12.86	20.61	s
	EPM7064S	4.62	4.67	4.81	5.05	5.53	6.97	9.37	14.17	s
	EPM7032S	4.33	4.37	4.47	4.63	4.96	5.96	7.62	10.95	s
MAX 7000A	EPM71024A	3.07	3.19	3.54	4.13	5.32	8.87	14.78	26.61	s
	EPM7512A	3.01	3.07	3.25	3.54	4.14	5.92	8.88	14.81	s
	EPM7384A	3.00	3.04	3.17	3.40	3.84	5.18	7.41	11.87	s
	EPM7256A	6.57	6.71	7.13	7.82	9.20	13.35	20.27	34.11	s
	EPM7128A	5.19	5.27	5.50	5.89	6.66	8.99	12.86	20.61	s
	EPM7064A	2.96	2.97	2.99	3.02	3.09	3.30	3.65	4.35	s
	EPM7032A	2.95	2.96	2.97	2.99	3.02	3.13	32.30	3.65	s

Table 3. Stand-Alone Verification Times for Different Test Clock Frequencies (Part 1 of 2)

Device Family	Device	f_{TCK}								Units
		10 MHz	5 MHz	2 MHz	1 MHz	500 kHz	200 kHz	100 kHz	50 kHz	
MAX 9000	EPM9560, EPM9560A	0.26	0.36	0.68	1.21	2.26	5.43	10.71	21.26	s
	EPM9480, EPM9480A	0.25	0.35	0.64	1.13	2.12	5.06	9.97	19.78	s
	EPM9400	0.24	0.33	0.61	1.06	1.97	4.69	9.23	18.30	s
	EPM9320, EPM9320A	0.24	0.32	0.57	0.99	1.82	4.32	8.49	16.82	s
MAX 7000S	EPM7256S	0.12	0.20	0.46	0.89	1.75	4.33	8.63	17.23	s
	EPM7192S	0.10	0.16	0.36	0.70	1.37	3.39	6.75	13.47	s
	EPM7160S	0.10	0.17	0.39	0.75	1.47	3.64	7.25	14.47	s
	EPM7128S	0.08	0.12	0.27	0.51	0.99	2.43	4.83	9.63	s
	EPM7064S	0.06	0.08	0.17	0.32	0.61	1.49	2.95	5.87	s
	EPM7032S	0.05	0.07	0.12	0.22	0.42	1.02	2.01	3.99	s

Table 3. Stand-Alone Verification Times for Different Test Clock Frequencies (Part 2 of 2)

Device Family	Device	f_{TCK}								Units
		10 MHz	5 MHz	2 MHz	1 MHz	500 kHz	200 kHz	100 kHz	50 kHz	
MAX7000A	EPM71024A	0.12	0.18	0.36	0.66	1.26	3.05	6.04	12.02	s
	EPM7512A	0.09	0.12	0.21	0.36	0.66	1.56	3.06	6.06	s
	EPM7384A	0.08	0.11	0.17	0.29	0.51	1.19	2.31	4.56	s
	EPM7256A	0.12	0.20	0.46	0.89	1.75	4.33	8.63	17.23	s
	EPM7128A	0.08	0.12	0.27	0.51	0.99	2.43	4.83	9.63	s
	EPM7064A	0.06	0.07	0.08	0.10	0.13	0.24	0.41	0.76	s
	EPM7032A	0.06	0.06	0.07	0.08	0.10	0.15	0.24	0.42	s

Figures 1, 2, and 3 show the in-system programming times versus f_{TCK} for MAX 9000 and MAX 7000S devices, respectively.

Figure 1. MAX 9000 In-System Programming Times vs. f_{TCK}

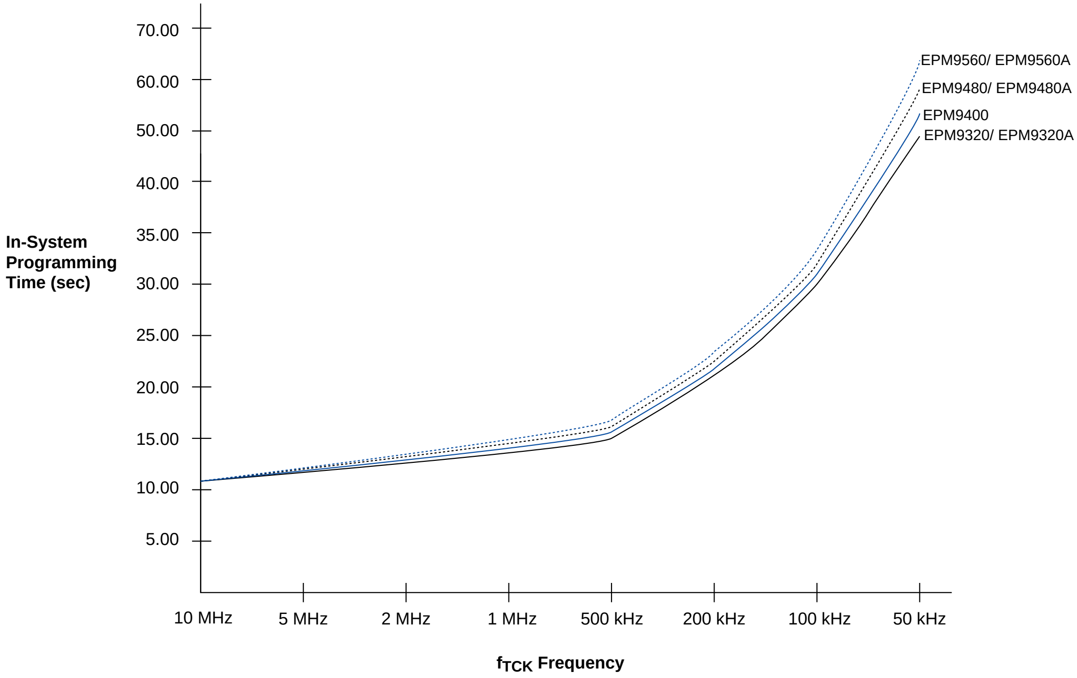


Figure 2. MAX 7000A In-System Programming Times vs. f_{TCK}

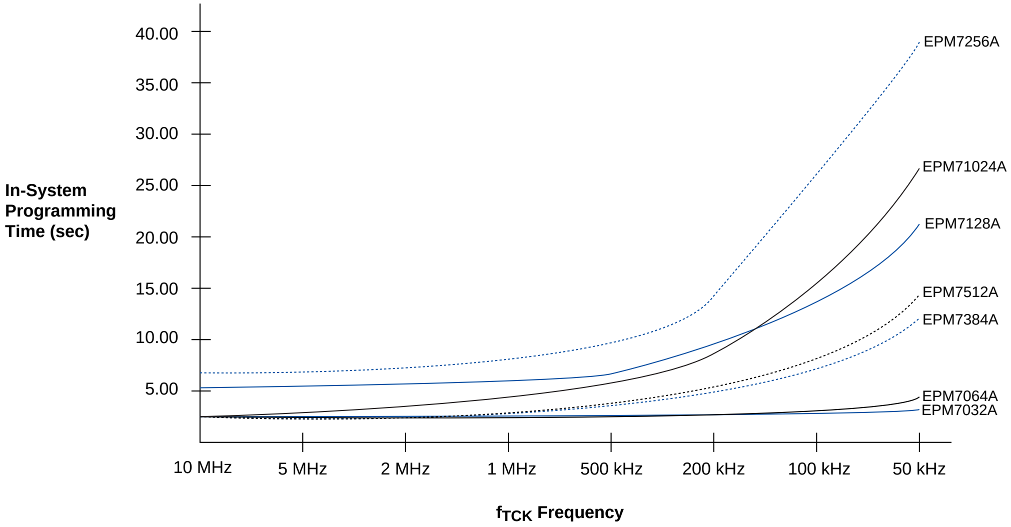
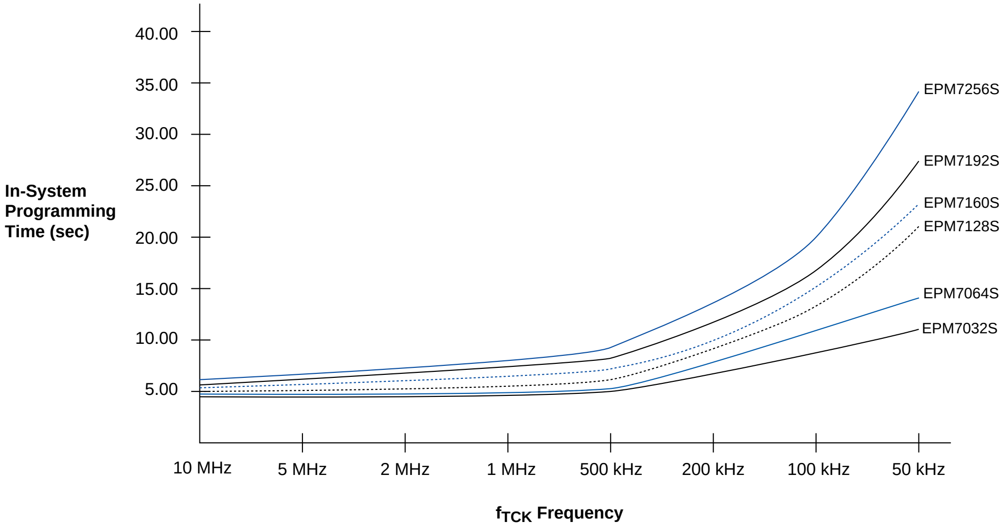


Figure 3. MAX 7000S In-System Programming Times vs. f_{TCK}



Programming Multiple Devices Concurrently

Devices in an IEEE 1149.1 JTAG chain can be programmed sequentially. However, ISP in Altera devices allows devices within the same family to be programmed concurrently, which can significantly reduce programming times. During concurrent programming, data is serially shifted to multiple devices along the JTAG chain and then programming pulses are applied simultaneously to all the devices. The time required to concurrently program multiple devices in a single family can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \sum_{\text{All Devices}} \frac{Cycle_{PTCK}}{f_{TCK}}$$

where: t_{PROG} = Programming time

t_{PPULSE} = Sum of the fixed times to erase, program, and verify the EEPROM cells for only the largest device

$Cycle_{PTCK}$ = Number of TCK cycles to program each device

f_{TCK} = TCK frequency

Table 4 shows the concurrent programming times for 1, 2, 10, and 100 devices in a JTAG chain.

Table 4. Concurrent Programming Times (Part 1 of 2)

Device Family	Device	Concurrent Programming Times *Note (1)*				Units
		1 Device	2 Devices	10 Devices	100 Devices	
MAX 9000	EPM9560, EPM9560A	12.25	12.49	14.43	36.24	s
	EPM9480, EPM9480A	12.05	12.27	14.07	34.26	s
	EPM9400	11.85	12.06	13.70	32.24	s
	EPM9320, EPM9320A	11.65	11.84	13.34	30.21	s
MAX 7000S	EPM7256S	6.57	6.71	7.82	20.27	s
	EPM7192S	5.82	5.93	6.80	16.60	s
	EPM7160S	5.47	5.57	6.30	14.61	s
	EPM7128S	5.19	5.27	5.89	12.86	s
	EPM7064S	4.62	4.67	5.05	9.37	s
	EPM7032S	4.33	4.37	4.63	7.62	s

Table 4. Concurrent Programming Times (Part 2 of 2)

Device Family	Device	Concurrent Programming Times *Note (1)*				Units
		1 Device	2 Devices	10 Devices	100 Devices	
MAX 7000A	EPM71024A	3.07	3.19	4.13	14.78	s
	EPM7512A	3.01	3.07	3.54	8.88	s
	EPM7384A	3.00	3.04	3.40	7.41	s
	EPM7256A	6.57	6.71	7.82	20.27	s
	EPM7128A	5.19	5.27	5.89	12.86	s
	EPM7064A	2.96	2.97	3.02	3.65	s
	EPM7032A	2.95	2.96	2.99	3.30	s

Note:

(1) Times are provided for devices programmed at 10 MHz.

Bypassing Devices Not Targeted for ISP

When programming devices in a chain of JTAG-capable devices, some of the devices may not be targeted for in-system programming. You can bypass the devices not targeted for ISP using the JTAG BYPASS instruction. The additional clock cycles required to shift in these bypass instructions are negligible when operating at frequencies higher than 100 kHz, and thus do not need to be considered.

Programming Methods

The importance of ISP programming times depends on the method used to program the device.

Prototyping via the MAX+PLUS II Software & Download Cables

During the development and prototyping stage of a design cycle, you can use ISP to make design iterations in minutes. In this configuration, programming times are not as critical as the ability to reprogram the device in-system. You can program an ISP-capable device via the MAX+PLUS® II software and the ByteBlaster™ download cable from the parallel port of a PC at 100 to 300 kHz. The MAX+PLUS II software also provides programming support for the BitBlaster™ download cable through the RS-232 port of either a PC or UNIX workstation at approximately 50 kHz. At these rates, the programming times of “F” versus non-“F” devices are identical. That is, any difference in the t_{PPULSE} and t_{VPULSE} terms are dominated by

$$\frac{Cycle_{PTCK}}{f_{TCK}}.$$

Production ISP via In-Circuit Testers

During the production stage, programming in-system via the JTAG interface allows manufacturing to incorporate device programming times into standard test flows. In this environment, in-system programming times are critical; the programming times directly impact the manufacturing costs per board. The f_{TCK} of in-circuit testers varies by manufacturer from 500 kHz to 10 MHz. At these rates, the programming times are primarily a function of the pulse widths. Altera recommends using MAX 9000 and MAX 7000S "F"-devices for short and consistent programming times. For information on the flow that is recommended for your specific in-circuit testers platform, contact Altera Applications at (800) 800-EPLD.

In-Field Upgrades via Embedded Processor

After a design has been shipped, you can change the design in an ISP-capable device with an embedded processor. The embedded processor transfers programming data from one memory source to the device. The embedded processor you select determines the time required to program the device in-system. The f_{TCK} of embedded processors varies from 10 kHz to 10 MHz.

Conclusion

In-system programming and verification times for MAX 9000, MAX 9000A, MAX 7000S, and MAX 7000A devices depend on three factors: the programming pulse width, the verify pulse width, and the test clock frequency. With high throughput, the time required to shift data in and out of these devices becomes negligible, and the programming and verification pulse times dominate the total ISP time. In-circuit testers supporting fast throughput rates (e.g., JTAG TCK = 10 MHz) can be employed to program the largest of these devices in less than five seconds.